Vivekananda College of Engineering & Technology, Puttur

[A Unit of Vivekananda Vidyavardhaka Sangha Puttur ®]

Affiliated to VTU, Belagavi & Approved by AICTE New Delhi

CRM08 Rev 1.10 CSE 13/02/2021

CONTINUOUS INTERNAL EVALUATION- 3

Dept:CSE	Sem / Div: 3/A&B	Sub:Computer Organization	S Code:18CS34				
Date:16/02/2021	Time: 2:30-4:00	Max Marks: 50	Elective:N				
Note: Answer any 2 full questions, choosing one full question from each part.							

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	Q N	Questions	Marks	RBT	COs		
	PART A						
1		Write down the steps of booth multiplication algorithm. Perform booth multiplication between (+13)*(-6)	10	L3	CO4		
	1	Write down the steps of non restoring division algorithm. Apply non restoring division algorithm on 18/7	10	L3	CO4		
	c	Explain with a neat figure the circuit arrangement for binary division	5	L3	CO4		
	OR						
2	a	Using sequential multiplication, multiply 22*10	10	L3	CO4		
	1	Write down the steps of restoring division algorithm. Apply restoring division algorithm on 25/4	10	L3	CO4		
	c	Using bit pair recoding multiply (+13)*(-6)	5	L3	CO4		
	PART B						
3		Discuss with a neat diagram, the single bus organization of the data path inside a processor	10	L2	CO3		
	b	Explain three bus organization of data path with a neat block diagram	10	L2	CO3		
	1	Write the control sequence for instruction Add R4, R5, R6 for 3 bus organization	5	L3	CO3		
	OR						
4	a	Explain Hard Wired Control unit organization in a processing unit	10	L2	CO3		
	1	What do you mean by micro instruction? Design basic organization of a micro programmed control unit with diagram.	10	L2	CO3		
		Write the control sequence for the execution of the instruction Add (R3),R1 in the execution of a complete instruction	5	L3	CO3		